Introduction to Computer Architecture

Assignment 2

Due November 26, 2018

1. [10 = 2 x 5]

Which is the code sequence for C = A + B for load-store ISA?

A.
```
Push A
Push B
Add
Pop C
```

B.
```
Load A
Add B
Store C
```

C.
```
Load R1, A
Add R3, R1, B
Store R3, C
```

D.
```
Load R1, A
Load R2, B
Add R3, R1, R2
Store R3, C
```

Which of the following is NOT an operation of ID stage?

A. A <- Regs[rs] B. B <- Regs[rt]

C. ALUOutput <- A + IMM D. IMM <- sign-extended immediate field of IR

Which operation does Add R1, @(R3) enforce?

A. Regs[R1] <- Regs[R1] + Regs[R3]

B. Regs[R1] <- Regs[R1] + Mem[Regs[R3]]

C. Regs[R3] <- Regs[R1] + Mem[Regs[R3]]

D. Regs[R1] <- Regs[R1] + Mem[Mem[Regs[R3]]]

In the following codes, there exist _____ data dependences.

```
ADD   R3, R2, R1
SUB   R2, R4, R3
SW    R2, #8(R4)
```

A. RAW, WAR B. RAW, WAW C. RAW, WAR, WAW D. WAR, WAW

Which sequence of instructions cannot use forwarding path to address all potential data hazards?

A.
```
Lw R1, 0(R2)
And R6, R1, R7
Or R8, R1, R9
```

B.
```
Lw R1, 0(R2)
Sub R6, R2, R7
Or R8, R6, R9
```

C.
```
Add R1, R2, R3
Lw R4, 0(R1)
```

D.
```
Add R1, R2, R3
SD R4, 12(R1)
```

2. [6 = 2 x 3]

For each of R, I, J type instructions:

a. draw its encoding format with each field marked;

b. explain the meanings of each field.

3. [10 = 2 x 5]

Based on the following pipeline datapath, draw the links taken by each instruction:

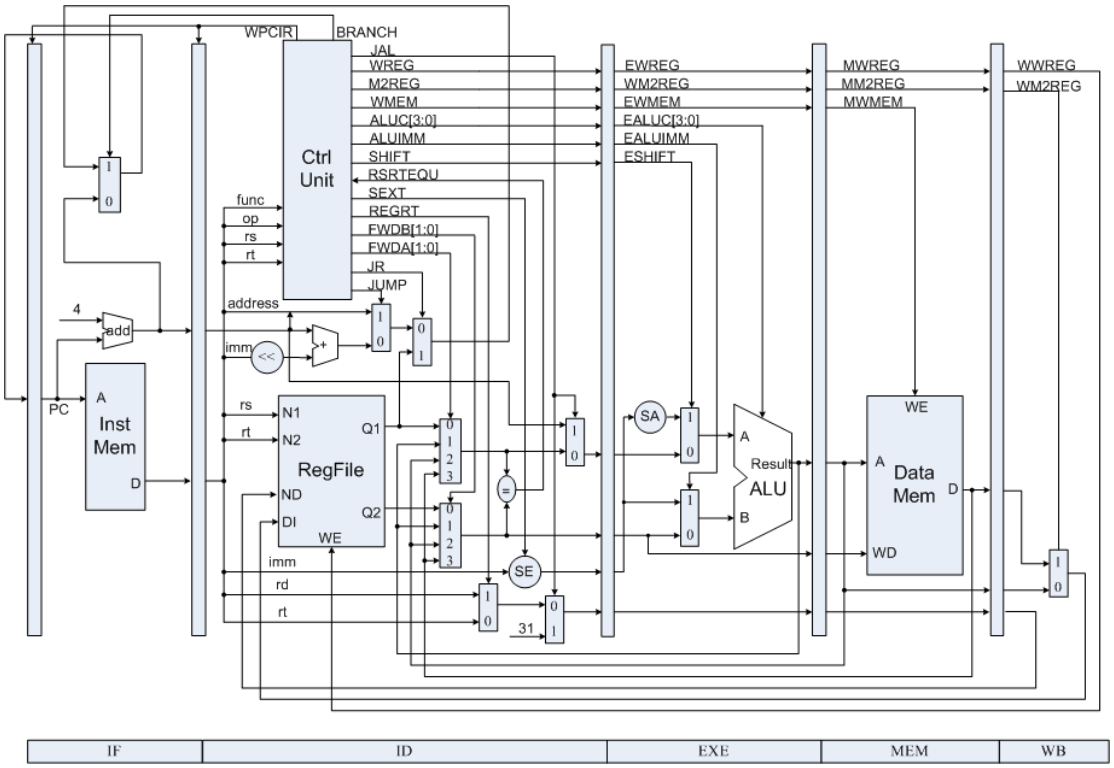
ADD

Load

Store

BNE

J



4. [4]

Analyze why ideal pipelining with equal-length pipe stages yields the highest speedup.

5. [10 = 5 x 2]

Reason about the following two penalties:

a. PredictedUntaken-PenaltyUntaken0;

b. PredictedTaken-PenaltyTaken2.

Branch scheme	Penalty unconditional	Penalty untaken	Penalty taken
Flush pipeline	2	3	3
Predicted taken	2	3	(2)
Predicted untaken	2	(0)	3

6. [10 = 5 x 2]

Use the following code fragment:

```
Loop:   LD      R1, 0(R2)       ; load R1 from address 0+R2
        DADDI   R1, R1, #1      ; R1 = R1 + 1
```

```
SD      R1, 0(R2)      ; store R1 at address 0+R2
DADDI   R2, R2, #4     ; R2 = R2 + 4
DSUB    R4, R3, R2     ; R4 = R3 - R2
BNEZ    R4, Loop       ; branch to Loop if R4 != 0
```

a. Assume that the initial value of R3 is R2 + 396.

Data hazards are caused by data dependences in the code. List all of the data dependences in the code above. Record the register, source instruction, and destination instruction; for example, there is a data dependency for register R1 from the LD to DADDI, that is,

R1 LD DADDI

b. Show the time of this instruction sequence for the 5-stage RISC pipeline with full forwarding and bypassing hardware. Use a pipeline timing chart like that shown in Figure C.5. Assume that the branch is handled by predicting it as not taken. If all memory references take 1 cycle, how many clock cycles does this loop take to execute?

7. [4 = 2 x 2]

You are designing a system for a real-time application in which specific deadlines must be met. Finishing the computation faster gains nothing. You find that your system can execute the necessary code, in the worst case, twice as fast as necessary.

a. How much energy do you save if you execute at the current speed and turn off the system when the computation is complete?

b. How much energy do you save if you set the voltage and frequency to be half as much?

8. [16 = 4 x 4]

For the following assume that values A, B, and C reside in memory. Also assume that instruction operation codes are represented in 8 bits, memory addresses are 64 bits, and register addresses are 6 bits.

For each instruction set architecture shown in Figure A.2 (*stack*, *accumulator*, *register-memory*, *register-register*), how many addresses, or names, appear in each instruction for the code to compute C = A + B, and what is the total code size?

9. [10 = 5 x 2]

Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache. Assume the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle, and there are 1.5 memory references per instruction.

a. What is the average memory access time and

b. average stall cycles per instruction?

Ignore the impact of writes.

10. [10 = 5 x 2]

Assume a fully associative write-back cache with many cache entries that starts empty.

Below is a sequence of five memory operations (the address is in square brackets):

```
Write   Mem[100];
Write   Mem[100];
Read    Mem[200];
Write   Mem[200];
Write   Mem[100];
```

What are the number of hits and misses (and which are them) when using no-write allocate versus write allocate?

11. [10] Dear All,

I hope you really enjoyed the class (at least for some moments) so far. You can't get to hear classmates rap and sing, eat chocolate and dztz in every class, right?

I am quite impressed with your overall performance. Alongside many other evidences are the concentration and interaction you dedicated in class, the confidence and English proficiency you showed in presentation, the collaboration and fraternity you built in lab, and the humor and joy you shared in QQ-group. For students taking the research practice, I really enjoyed all our meetings and discussions. You kept amazing me with your greater potential. Even though some may have played mobile games or fallen asleep in class, you still managed to guarantee a constant high attendance rate. This, in turn, motivates and encourages me to keep improving my teaching skills.

How to make the most of your attendance in class? As I occasionally mentioned in previous lecture sessions, I sincerely hope that you could try to follow slides on the projector screen instead of your computers/smartphones. Why? Can you imagine what I felt each time I saw some of you staring at your computers/smartphones (or even desks)? Sometimes, it was really challenging to feel pumped up when my inner voice questioned the necessity of my interpretation of the slides. I felt like even if I was simply mumbling and you would not even notice or care. Surely I have no rights to regulate your behaviors in any situation. And I could've simply focused on the students following my lead. Then why I still insist on trying to make teaching attractive and interesting through, for example, crafting slide design and organization, rehearsing corresponding presentation, and experimenting likely fun activities?

As students, you are always the reason. You decided to study Computer Architecture with me among several instructors. I truly appreciate your trust and support. Ever since we met, I keep working on how to provide you with a satisfactory learning experience in return. Again, why am I suggesting you to follow slides on the projector screen instead of your computers/smartphones (and also suggesting you not to preview slides before class)? This is because it likely increases the chances for you to grasp the essence of the teaching content. How? You may wonder. I have attempted to organize the content on each slide deck into a series of logically progressive questions.

It has been my hope that this helps to create a conversational teaching style. Consider when you are chatting with your friend. Have you ever simply listened to her or him for two or three 45-mins without interruption? Presumably (if you are not a dztz and care at least a little bit of your conversation with your friend), the answer is no. Then that's exactly what I think we should follow in class. I expect you to take initiative to make the class more interactive (and hopefully more interesting). May it be raising a question or answering a question I asked. We can thus ensure that we are on the same page with the teaching content. With the slides, my interpretation, and our interaction, I believe that together we can improve the odds of knowing not only how but also why. Knowing not only how a strategy works but also why it works in its own way instead of some other ways, I think, is the ultimate goal of taking any course. The design rationale behind it may benefit problem solving and decision making in work and life.

So, please take more initiative in class. Wouldn't it be great if we could create an atmosphere in class like what we have in QQ-group?

At least, give it a try.

??With this question, I would like you to express your thoughts and feelings of this course so far. For example, did you gradually understand strategies or things from different perspectives and weight their tradeoffs? What do you think is the real challenge for you to learn this course? Do you consider interactions in class helpful? What held you back when you were trying to ask or answer questions in class? What suggestions (for better learning this course) would you like to provide to other students? What help or assistance would like from me or other students? What else?

Thank you for everything and look forward to hearing you out. Have fun.