Introduction to Computer Architecture

Quiz 1

May 21, 2015

1. [10] Assume a disk subsystem with the following components and MTTF:

- 10 disks, each rated at 1,000,000-hour MTTF;
- 1 ATA controller, 500,000-hour MTTF;
- 1 power supply, 200,000-hour MTTF;
- 1 fan, 200,000-hour MTTF;
- 1 ATA cable, 1,000,000-hour MTTF;

Using the simplifying assumptions that the lifetimes are exponentially distributed and the failures are independent, compute the MTTF of the system as a whole.

2. [10 = 5 + 5] What operations do the following instruction indicate?

a. Add R4, 100(R1)
b. Add R1, @(R3)

3. [10 = 2 x 5] Which are the five stages of the classic five-stage pipeline for a RISC processor? What operations does each stage perform?

4. [20 = 10 + 10] Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache. Assume the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle, and there are 1.5 memory references per instruction.

a*. What is the average memory access time and*
b. *average stall cycles per instruction?*

Ignore the impact of writes.

5. [10] Use the following code fragment:

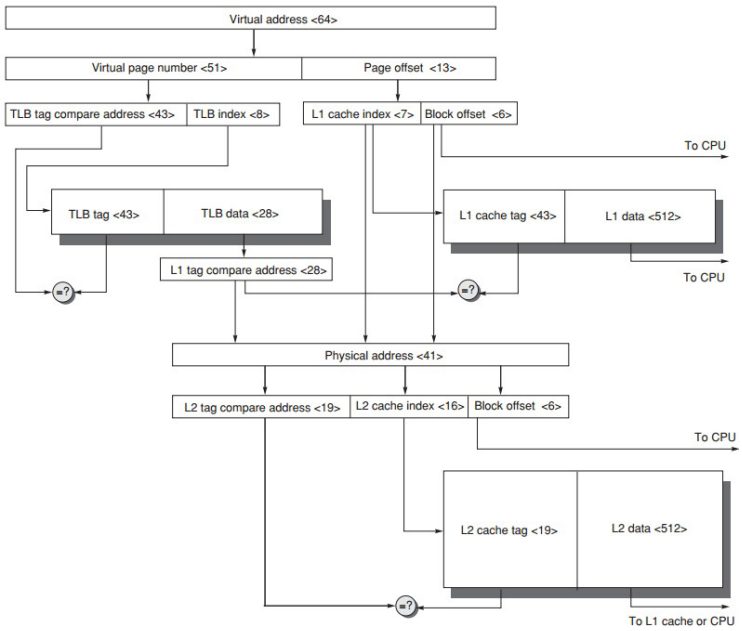
```
Loop:   LD      R1, 0(R2)       ; load R1 from address 0+R2
        DADDI   R1, R1, #1      ; R1 = R1 + 1
        SD      R1, 0, (R2)     ; store R1 at address 0+R2
        DADDI   R2, R2, #4      ; R2 = R2 + 4
        DSUB    R4, R3, R2      ; R4 = R3 - R2
        BNEZ    R4, Loop        ; branch to Loop if R4 != 0
```

Assume that the initial value of R3 is R2 + 396.

Data hazards are caused by data dependences in the code. List all of the data dependences in the code above. Record the register, source instruction, and destination instruction; for example, there is a data dependency for register R1 from

the LD to DADDI, that is,
R1 LD DADDI

6. [10] Describe the address translation process on the following memory system.



7. [20 = 10 x 2] For the code below, assume we have an 8 KB direct-mapped data cache with 16-byte blocks, and it is a write-back cache that does write allocate. The elements of a and b are 8 bytes long since they a double-precision floating-point arrays. There are 3 rows and 100 columns for a and 101 rows and 3 columns for b. Assume they are not in the cache at the start of the program.
Determine the number of cache misses and which accesses cause them for the following codes with or without prefetching.

```
for (i = 0; i < 3; i = i+1)
        for (j = 0; j < 100; j = j+1)
                a[i][j] = b[j][0] * b[j+1][0];
```

```
for (j = 0; j < 100; j = j+1) {
        prefetch(b[j+7][0]);
        /* b(j,0) for 7 iterations later */
        prefetch(a[0][j+7]);
        /* a(0,j) for 7 iterations later */
        a[0][j] = b[j][0] * b[j+1][0];};
for (i = 1; i < 3; i = i+1)
        for (j = 0; j < 100; j = j+1) {
                prefetch(a[i][j+7]);
                /* a(i,j) for +7 iterations */
                a[i][j] = b[j][0] * b[j+1][0];}
```

8. [10] Design a question that you think is feasible as an exam question.
1) which topic you would like to consider?
2) describe the question;
3) provide also the sample solution.