College of Computer Science, Zhejiang University

Introduction to Computer Architecture

Spring Semester, 2012-2013

Lecture time: Monday, 1:15pm–3:20pm, in West-CaoGuangBiao 101

Lab time: Monday, 3:30pm–5:30pm, in West-CaoGuangBiao 310

Instructor:

- **Jiang Xiaohong**

Office: Room 520, Cao GuangBiao Building in YuQuan campus.

Office time: 2:00pm—4:00pm, Tuesday

Mobile: 13396550102

Email: jiangxh@zju.edu.cn

Homepage: http://www.cs.zju.edu.cn/people/jiangxh

CoureWebsite: http://10.71.45.100/

http://www.cs.zju.edu.cn/people/jiangxh/EliteCourse/index.html

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Objective:

This course is one of the most important professional courses in computer science that systemically introduce the fundamental concepts and design approches of computer architecture from the view of the whole computer system. The topics cover fundamental concepts, task of computer design, quantitative principles, and performance evaluation; instruction set architecture and characteristics of CISC and RISC machines; basic concepts for pipelining, causes and resolutions for pipeline hazards; memory hierarchy, improvement of cache performance; I/O storages; and basic concepts for multiprocessors. At the same time, the students are required to master the hardware design approches and skillfully use hardware design toolkits. In the lab we will introduce how to gradually implement the pipelined CPU supporting 31 MIPS instructions in Xilinx ISE environment using Verilog, and verify its correctness on FPGA board.

Textbook:

- **Computer Architecture - A Quantitative Approach (4th edition)**

John L. Hennessy and David A. Patterson

China Machine Press

•**Computer Architecture - A Quantitative Approach (3rd edition) (Chinese Version)**

Translated by Zheng, Weimin(郑纬民等） etc.

Publishing House of Electronics Industry

Prerequisites:

Computer Organization, Assemble Language, Operating System

Topics:

Introduction to the course (1 credit-hour)

Chapter 1：Fundamentals of Computer Design (5 credit-hours)

1.1 Introduction

1.2 Classes of Computers

1.3 Defining Computer Architecture

1.4 Trends in Technology

1.5 Trends in Power in integrated circuits

1.6 Trends in cost

1.7 Dependability

1.8 Measuring, reporting and summarizing performance

1.9 Quantitative principles of computer design

1.10 Performance and price-performance

1.11 Answer to assignments

Chapter 2：Instruction Set Principles and Examples (5 credit-hours)

2.1 Introduction

2.2 Classifying instruction set architecture

2.3 Memory addressing

2.4 Type and size of operands

2.5 Operation in the instruction set

2.6 Instruction s for control flow

2.7 Encoding an instruction set

2.8 The role of compilers

2.9 The MIPS architecture

2.10 Answer to assignments

Chapter 3：Pipelining: Basic and Intermediate Concepts (12 credit-hours)

3.1 Introduction

3.2 The Major hurdles of pipelining-pipeline hazards

3.3 How is pipelining implemented ?

3.4 What makes pipelining hard to implement?

3.5 Extending the MIPS pipeline to handle multicycle operations

3.6 The MIPS R4000 pipeline

3.7 Survey of Instruction Level Parallelism

3.8 Answer to assignments

Chapter 4 ： Memory Hierarchy Design 10 hours

4.1 Introduciton

4.2 Cache performance

4.3 Six Basic cache optimizations

4.4 Eleven advanced optimizations of cache performance

4.5 Memory technology and optimizations

4.6 Virtual memory

4.7 Protection and examples of virtual memory

4.8 Virtual memory and virtual machines

4.9 The design of memory hierarchies

4.10 AMD opteron memory hierarchy

4.11 Answer to assignments

Chapter 5： Multiprocessors (2 credit-hours)

5.1 Introduciton

5.2 Symmetric Shared-Memory Architecture

5.3 Performance of Symmetric Shared-Memory Architecture

5.4 Distributed shared memory and directory-based coherence

Chapter 6：Perspective of computer architecture (2 credit-hours)

Overview of the course：(3 credit-hours)

Lab:

·Object

Learn the operation of Spartan3E Board and the usage of ISE. Understand the principle of the pipelined CPU and MIPS instructions. Design the pipelined CPU that can execute 31 MIPS instructions correctly on Spartan3E board step by step according to the project tutorial.

·Schedule

Lab 1). Warmup based you lab work in the course “computer organization”. To learn the Spartan 3E board, review the ISE environment, and try to updating your verilog code of the display part of multiple-cycle CPU to make it run correctly on 3E

board. Try to add one new branch instruction.

Lab 2). Implement 5-stage pipelined CPU with 15 MIPS instructions (only required to execute in pipeline).

Lab 3). Implementing "stall" when have hazards so that CPU can execute program correctly.

Lab 4). Implementing “forwarding paths” to make CPU run faster.

Lab 5). Adding the other 16 instructions and implementing total 31 MIPS instructions in your pipelined CPU, which solves control hazard with predict-not-taken policy.

- **Grading**

  1) Participating: 4%

  2) Lab1-5: 4%, 6%, 5%, 5%, 8%

  Note: Each lab consists of two parts: the lab result and lab report. The experiment is encouraged to be done **individully**, and the lab result is required to be submitted to the course website.

- **Lab report submission:**

  Submit your lab report to the course website into the lab directory naming in StID_name_lab1.doc, …, StID_name_lab4.doc, and **StID_name_lab5.rar** including StID_name_lab5.doc **and your lab work directory**.

  Submission deadline will be announced on course website.

Homework:

- Total 4 times, once per chapter
- Submission deadline will be normally one week after assigned, and will be announced on **course website**.
- For doing homework, discussion is greatly encouraged, but every student is required to **Do and Submit** the homework individually on time.

Submission rule and late policy:

- All assignments are required to be written in English.
- All assignments are required to be submitted in time to the appointed directory on the course site.
- Please name your submitted document as “StID_Name_hw1.doc”.
- Three day late submission will get 10% off from grading; Six day late homework will get 20% off from grading.
- Late assignments **more than Six days** are **NOT** acceptable.

Grading:

- 4%: Class participation & performance
- 16%: Homework
- 8%: Pop quiz
- 32%: Lab assignments (4%participation, 4%, 6%, 5%, 5%, 8%)
- 40%: Final examination (close-book paper test)
- **Bonus1: 5%**: Submit a review with PPT file for literature reading
- **Bonus2: <=5%**: **Active performance in the class** is highly encouraged with bonus, such as asking good question or answering the question correctly in the class, adding 1% each time.

Bonus: Literature reading (5%):

- Find one paper (**no less than 8 pages**) in English **in recent three years** on top conferences or international journals in computer architcture. The list of international conferences and journals will be uploaded on the course website.
- Read the paper and then **write a review** including 1) Why: what problem proposed. You can find it in the section of introduction; 2)What: what have been done in this area. You can find it in the section of related work; 3)How: what approaches are the auther used to solve the problem. How well ? The most important part of the paper including experiments and results. 4) Your opinions: existing problems, what else has not been noted, inspired ideas, or … .
- The review is required within 3 A4 pages in 11th Times New Romar fond with a 1.5 line space, including an abstract both in English (150-200 words) and in Chinese (5th font) by yourself.
- **Prepare a PPT** file of 25-30 pages **With Notes** try to introduce the contents of the paper in 20 minutes.
- The reading assignment need to be submitted in RAR file named **StID_name_read.rar** including StID_name_review.doc with abstract, StID_name_pre.ppt, and the **original paper**.
- Reading grading: 75%(review) + 25%(ppt).
